AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 4, 6, 7, 17, 19, 20, 23, 32, 35, 38, 40, 41, 44 and 45 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method of creating a model of a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said method comprising the steps of:

conducting a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said at least one surrounding circuit using a subsystem circuit model and a model of said at least one surrounding circuit;

recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing said test sequence of data processing operations; ~~and~~

generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change; and

using at least a representation of said recorded input signals to form a reduced model to replay said recorded input signals to said subsystem circuit model and to apply ~~a~~said plurality of non cycle-based sampling rules to said output signals to sample said output signals to detect

changes and times of changes in said output signals and to compare said output signals with at least one predetermined characteristic indicative of correct operation;

whereby said subsystem model and said reduced model simulate said subsystem performing said test sequence of data processing operations without simulating operation of said at least one surrounding circuit.

2. (previously presented) A method as claimed in claim 1, wherein formation of said reduced model uses at least one configuration file including data specifying input signals to said subsystem circuit, output signals from said subsystem circuit and bi-directional signals exchanged with said subsystem circuit.

3. (original) A method as claimed in claim 2, wherein signals from said subsystem are used to determine when bi-directional signals can be driven making allowance for variations in delays inherent in output loads.

4. (currently amended) A method as claimed in claim 1, wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation and wherein any change in said output signal is monitored throughout said time window.

5. (original) A method as claimed in claim 4, wherein said predetermined output signal value is one of: high; low; changed; and high impedance.

6. (currently amended) A method as claimed in claim 1, wherein within said data processing apparatus at least one of said output signals other than a repetitive clock signal is a strobe output signal used to trigger sampling of at least one strobed output signal, said reduced model including a rule whereby a change in said strobe output signal is detected and used to verify the correct state of said at least one strobed output signal.

7. (currently amended) A method as claimed in claim 6, wherein said rule includes a strobe output signal time window within which a change in said strobe output signal to a predetermined strobe output signal value should occur to be indicative of correct operation, and wherein any change in said strobe output signal is monitored throughout said time window.

8. (original) A method as claimed in claim 6, wherein said rule includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation.

9. (original) A method as claimed in claim 8, wherein said strobed output signal time window is non-symmetrically disposed about a time when said strobed output signal is sampled.

10. (original) A method as claimed in claim 8, wherein said strobed output signal time window is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change.

11. (original) A method as claimed in claim 10, wherein said settling time window is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change.

12. (previously presented) A method as claimed in claim 1, wherein said full subsystem circuit model from which said input signals and said output signals are recorded is different from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed.

13. (original) A method as claimed in claim 12, wherein said full subsystem circuit model may change between different versions during regression testing.

14. (original) A method as claimed in claim 12, wherein said full subsystem circuit model may change between being one of an RTL model, a netlist model or other software view.

15. (previously presented) A method as claimed in claim 1, wherein changes in at least one of said output signals other than at sampling instants of a corresponding one of said sampling rules for that output signal are also monitored.

16. (original) A method as claimed in claim 1, comprising recording progress messages for replay during regression testing.

17. (currently amended) Apparatus for creating a model of a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said apparatus comprising:

logic hardware for conducting a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said at least one surrounding circuit using a subsystem circuit model and a model of said at least one surrounding circuit;

logic hardware for recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing said test sequence of data processing operations;

logic hardware for generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change;

logic hardware, using at least a representation of said recorded input signals and one or more configuration files, for forming a reduced model to replay said recorded input signals to said subsystem circuit model and for applying ~~a~~said plurality of non cycle-based sampling rules to said output signals of said subsystem circuit model to sample said output signals to detect changes and times of changes in said output signal and to compare said output signals with at least one predetermined characteristic indicative of correct operation; and

whereby said subsystem model and said reduced model simulate said subsystem performing said test sequence of data processing operations without simulating operation of said at least one surrounding circuit.

18. (previously presented) A computer program embodied on a computer-readable medium and comprising computer readable code that, when executed,controls a computer to perform a method as claimed in claim 1.

19. (currently amended) A method of modelling a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said method comprising the steps of:

providing a subsystem circuit model and a reduced model, said reduced model having been formed by recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing a test sequence of data operations;

using said reduced model for generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change;

using said reduced model to apply a sequence of said recorded input signals to a model of said subsystem circuit, said input signals corresponding to those provided by said at least one surrounding circuit to said subsystem circuit when performing said test sequence of data processing operations; and

using said reduced model to apply a sampling rule associated with each output signal of said subsystem circuit to sample said output signal to detect changes and times of changes in said output signal and to compare said output signal with at least one predetermined characteristic indicative of correct operation.

20. (currently amended) A method as claimed in claim 19, wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation and wherein any change in said output signal is monitored throughout said time window.

21. (original) A method as claimed in claim 20, wherein said predetermined output signal value is one of: high; low; changed; and high impedance.

22. (original) A method as claimed in claim 19, wherein within said data processing apparatus at least one of said output signals is a strobe output signal used to trigger sampling of at least one strobed output signal, said reduced model including a rule whereby a change in said strobe output signal is detected and used to trigger sampling within said reduced model of said at least one strobed output signal.

23. (currently amended) A method as claimed in claim 22, wherein said rule includes a strobe output signal time window within which a change in said strobe output signal to a predetermined strobe output signal value should occur to be indicative of correct operation, and wherein said strobe output signal is monitored for change throughout said time window.

24. (original) A method as claimed in claim 22, wherein said rule includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation.

25. (original) A method as claimed in claim 24, wherein said strobed output signal time window is non-symmetrically disposed about a time when said strobed output signal is sampled.

26. (original) A method as claimed in claim 24, wherein said strobed output signal time window is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change.

27. (original) A method as claimed in claim 26, wherein said settling time window is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change.

28. (previously presented) A method as claimed in claim 19, wherein said full subsystem circuit model from which said input signals and said output signals are recorded is different from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed.

29. (original) A method as claimed in claim 28, wherein said full subsystem circuit model may change between different versions during regression testing.

30. (original) A method as claimed in claim 28, wherein said full subsystem circuit model may change between being one of an RTL model, a netlist model or other software view.

31. (previously presented) A method as claimed in claim 19, wherein changes in at least one of said output signals other than at sampling instants for that output signal are also monitored.

32. (currently amended) Apparatus for modelling a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said apparatus comprising:

logic hardware for providing a subsystem circuit model and a reduced model;

logic hardware, using said reduced model, for applying a sequence of previously recorded input signals to a model of said subsystem circuit, said previously recorded input signals having been recorded in response to changes in said input signals and said input signals corresponding to those provided by said at least one surrounding circuit to said subsystem circuit when performing a test sequence of data processing operations; ~~and~~

logic hardware, using said reduced model, for generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change; and

logic hardware, using said reduced model, for applying a ~~sampling rule~~corresponding one of said plurality of non cycle-based sampling rules associated with each output signal of said subsystem circuit to sample said output signal to detect changes and to record times of changes in said output signal and for comparing said output signal with at least one predetermined characteristic indicative of correct operation.

33. (previously presented) A computer program embodied on a computer-readable medium and comprising computer readable code that, when executed, controls a computer to perform a method as claimed in claim 19.

34. (previously presented) A computer program product comprising a computer readable medium containing computer readable instructions that when executed perform the method steps of the reduced model of claim 1.

35. (currently amended) A method of creating a model of a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said method comprising the steps of:

conducting a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said at least one surrounding circuit using a subsystem circuit model and a model of said one or more surrounding circuits;

recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing said test sequence of data processing operations; ~~and~~

generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change; and

using at least a representation of said recorded input signals to form a reduced model to replay said recorded input signals to said subsystem circuit model and to apply ~~a~~said plurality of non cycle-based sampling rules to said output signals to sample said output signals to detect changes and times of changes in said output model and to compare said output signals with at least one predetermined characteristic indicative of correct operation;

whereby said subsystem model and said reduced model are operable to simulate said subsystem performing said test sequence of data processing operations without simulating operation of said at least one surrounding circuit; and

wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation and wherein any change in said output signal is monitored throughout said time window.

36. (previously presented) A method as claimed in claim 35, wherein said predetermined output signal value is one of: high; low; changed; and high impedance.

37. (previously presented) A method as claimed in claim 35, wherein signals from said subsystem are used to determine when bi-directional signals can be driven making allowance for variations in delays inherent in output loads.

38. (currently amended) A method as claimed in claim 35, wherein within said data processing apparatus at least one of said output signals other than a repetitive clock signal is a strobe output signal used to trigger sampling of at least one strobed output signal, said reduced

model including a rule whereby a change in said strobe output signal is detected and used to verify the correct state of the output signal.

39. (previously presented) A method as claimed in claim 35, wherein changes in at least one of said output signals other than at sampling instants for that output signal are also monitored.

40. (currently amended) Apparatus for creating a model of a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said apparatus comprising:

logic hardware for conducting a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said at least one surrounding circuit using a subsystem circuit model and a model of said at least one surrounding circuit;

logic hardware for recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing said test sequence of data processing operations; ~~and~~

logic hardware for generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change; and

logic hardware using at least a representation of said recorded input signals and at least one configuration file for forming a reduced model to replay said recorded input signals to said

subsystem circuit model and to apply ~~a~~said plurality of non cycle-based sampling rules to said output signals of said subsystem circuit model to sample said output signals to detect changes and times of changes in said output signals and to compare said output signals with at least one predetermined characteristic indicative of correct operation;

whereby said subsystem model and said reduced model are operable to simulate said subsystem performing said test sequence of data processing operations without simulating operation of said at least one surrounding circuit, and wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation and wherein any change in said output is monitored throughout said time window.

41. (currently amended) Apparatus for modelling a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said apparatus comprising:

logic hardware providing a subsystem circuit model and a reduced model, said reduced model having been formed by recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing a test sequence of data processing operations;

logic hardware using said reduced model for applying said sequence of previously recorded input signals to a model of said subsystem circuit, said input signals corresponding to those provided by said at least one surrounding circuit to said subsystem circuit when performing a test sequence of data processing operations;

logic hardware using said reduced model for generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change;

logic hardware using said reduced model to apply a ~~sampling rule~~corresponding one of said plurality of non cycle-based sampling rules associated with each output signal of said subsystem circuit to sample said output signal to detect changes and times of changes in said output signal and comparing said output signal with at least one predetermined characteristic indicative of correct operation; and

wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation and wherein any change in said output signal is monitored throughout said time window.

42. (previously presented) A computer program product embodied on a computer-readable medium and comprising a computer readable code that, when executed, controls a computer to perform a method as claimed in claim 35.

43. (previously presented) A computer program product comprising a computer readable medium containing computer readable instructions that when executed perform the method steps of the reduced model of claim 35.

44. (currently amended) A method of creating a model of a data processing apparatus having a subsystem circuit under test and at least one surrounding circuit operable to provide input signals to and receive output signals from said subsystem circuit, said method comprising the steps of:

conducting a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said at least one surrounding circuit using a subsystem circuit model and a model of said at least one surrounding circuit;

recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals whilst performing said test sequence of data processing operations; ~~and~~

generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change; and

using at least a representation of said recorded input signals to form a reduced model to replay said recorded input signals to said subsystem circuit model and to apply ~~a~~said plurality of non cycle-based sampling rules to said output signals to sample said output signals to detect changes and times of changes in said output signals and to compare said output signals with at least one predetermined characteristic indicative of correct operation;

whereby said subsystem model and said reduced model simulate said subsystem performing said test sequence of data processing operations without simulating operation of said at least one surrounding circuit, wherein within said data processing apparatus at least one of said output signals other than a repetitive clock signal is a strobe output signal used to trigger

sampling of at least one strobed output signal, said reduced model including a rule whereby a change in said strobe output signal is detected and used to verify the correct state of said at least one strobed output signal.

45. (currently amended) A method as claimed in claim 44, wherein said rule includes a strobe output signal time window within which a change in said strobe output signal to a predetermined strobe output signal value should occur to be indicative of correct operation and wherein any change in said strobe output signal is monitored throughout said time window.

46. (previously presented) A method as claimed in claim 44, wherein said rule includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation.

47. (previously presented) A method as claimed in claim 46, wherein said strobed output signal time window is non-symmetrically disposed about a time when said strobed output signal is sampled.

48. (previously presented) A method as claimed in claim 46, wherein said strobed output signal time window is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change.

49. (previously presented) A method as claimed in claim 48, wherein said settling time window is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change.